REMARKS

Claims 1 - 6, and 8 are present in the subject application.

In the Office Action of October 29, 2008, the Examiner has rejected claims 1 – 6, and 8 under 35 U.S.C. §103(a). Reconsideration of the subject application is respectfully requested in view of the following remarks.

The Examiner has rejected claims 1 – 6, and 8 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 7,184,664 (Farmer et al.) in view of U.S. Patent Application Publication No. 2002/0063924 (Kimbrough et al.).

The Examiner takes the position that the Farmer et al. patent discloses the claimed subject matter, except for each downstream modulator being associated with at least one corresponding DHCT and having an identification number that is inserted into the forward signals, and one of the downstream modulators associated with the at least one DHCT for receiving the optical signals and for sending the forward signals. The Examiner further alleges that the Kimbrough et al. publication discloses these features, and that it would have been obvious to combine the Farmer et al. patent and Kimbrough et al. publication to attain the claimed invention.

This rejection is respectfully traversed. In particular, independent claim 1 recites the features of: at least one digital home communications terminal (DHCT) for receiving forward signals from a headend facility and for transmitting reverse RF signals to the headend facility; a single wire return device (SWRD) for receiving the reverse RF signals from the at least one DHCT, demodulating the reverse RF signals via an upstream demodulator, and converting the

demodulated signals to Ethernet signals; a plurality of downstream modulators located in the headend facility remote from the upstream demodulator with each downstream modulator associated with at least one corresponding DHCT and having an identification number that is inserted into the forward signals from the headend facility to identify that downstream modulator to the at least one corresponding DHCT, one of the downstream modulators associated with the at least one DHCT for receiving the optical signals and for sending the forward signals; the at least one DHCT inserting the modulator identification number received within the forward signals from the headend facility into the reverse header information; and the SWRD converting the modulator identification number within the reverse header information into an Internet Protocol address to enable the reverse signals to be directed to the one downstream modulator.

Independent claim 5 recites the features of: receiving forward signals from a headend facility and generating a reverse RF modulated signal in a digital host communications terminal (DHCT); a plurality of downstream modulators located in the headend facility with each downstream modulator associated with at least one corresponding DHCT and having an identification number that is inserted into the forward signals from the headend facility to identify that downstream modulator; the reverse RF modulated signal including the identification number of the downstream modulator associated with the DHCT in header information; demodulating the reverse RF modulated signal via an upstream demodulator remote from the plurality of downstream modulators to provide a reverse demodulated signal; processing the reverse demodulated signal to provide a reverse Ethernet signal, wherein the identification number is converted into an Internet Protocol address that enables the reverse Ethernet signal to

be directed to the associated downstream modulator; and receiving the reverse optical signal at the associated downstream modulator located in the headend facility, wherein the downstream modulator transmits a forward signal to the DHCT in response to the received reverse optical signal.

The Farmer et al. patent does not disclose, teach or suggest these features. Rather, the Farmer et al. patent discloses a return path system. The system includes inserting RF packets between regular upstream data packets, where the data packets are generated by communication devices, such as a computer or internet telephone. The RF packets can be derived from analog RF signals that are produced by legacy video service terminals. In this way, the system can provide an RF return path for legacy terminals that shares a return path for regular data packets in an optical network architecture (e.g., See Abstract).

The Examiner construes subscriber optical interface 140 of the Farmer et al. patent as the claimed single wire return device (SWRD), and further asserts that microprocessor 550, Data Interface 555 and selecting switch 513 of the Farmer et al. patent read on the claimed feature of converting the demodulated reverse RF signals to Ethernet signals.

However, subscriber optical interface 140 is coupled to a video services terminal 117 (construed by the Examiner as the claimed DHCT) that sends a reverse RF signal through a modulated RF signal I/O 535 to an RF diplexer 507. The diplexer 507 passes the reverse RF signal to an A/D converter 509. The converted RF signal is sent to a data reducer 511 that merely compresses the data, and subsequently to a data conditioner 407 acting as a buffer. The converted RF signal is further sent to a digital optical transmitter 530 only when switch 513 is

connected to the data conditioner 407 as controlled by microprocessor 550. The switch basically enables interleaving of the RF and regular data packets (e.g., See Fig. 8; and Column 21, lines 21 - 56). Accordingly, since the microprocessor 550 and the data interface 555 are never connected to the reverse RF signal path of video services terminal 117, the reverse RF signal from the video services terminal cannot be converted to Ethernet as recited in the independent claims.

In addition, there is no disclosure, teaching or suggestion of identifying a downstream modulator associated with at least one corresponding DHCT by having an identification number that is inserted into the forward signals from the headend facility to identify that downstream modulator to the at least one corresponding DHCT, wherein the at least one DHCT inserts the modulator identification number received within the forward signals from the headend facility into the reverse header information, and wherein the SWRD converts the modulator identification number within the reverse header information into an Internet Protocol address to enable the reverse signals to be directed to the one downstream modulator as recited in the independent claims. The Examiner concedes that the Farmer et al. patent does not disclose these features with respect to identifying a downstream modulator at Page 4 in the Office Action.

The Kimbrough et al. publication does not compensate for the deficiencies of the Farmer et al. patent. Rather, the Kimbrough et al. publication discloses a Fiber-to-the-Home (FTTH) multi-media access system and method in which voice, video and data signals are transported over a passive optical network (PON) between a central office location and a plurality of subscriber home network units (HNUs). Optical video distribution circuitry and telephony/data distribution circuitry at the central office location are included in the system and operate to send

and receive CATV video, PBS video television, telephony and Packet data signals to and from the HNUs via the PON. Optical multiplexing/demultiplexing circuitry operating at the central office combines the video signals, which are operating at one optical wavelength, with the telephony/data signals, which are operating at a second, distinct optical wavelength. These combined optical signals are then transported over the PON to the HNUs. The PON includes a plurality of distribution fibers coupled to a plurality of passive optical splitters, which are each coupled to a plurality of drop fibers that connect to the HNUs. The HNUs receive the combined optical signals, demultiplex and convert the optical signals into corresponding electrical signals, which are in turn coupled through the HNU to the video, data and telephony networks within the home. The HNUs also receive upstream electrical signals from devices within the home, multiplex and convert these electrical signals into upstream optical signals, and transmit these upstream optical signals to the central office (e.g., See Abstract).

The Examiner construes the HNU 50, Quad OIU card 20A and 10Base-T Ethernet PHY 54 of the Kimbrough et al. publication respectively as the claimed digital home communications terminal (DHCT), downstream modulator, and single wire return device (SWRD). The Examiner takes the further position that Quad OIU card 20A inserts its MAC address for reception by HNU 50, and that this address is inserted into the reverse signals and converted to an IP address by Ethernet PHY 54.

However, the Kimbrough et al. publication discloses that when a particular HNU 50 is attached to the system, the HNU 50 starts sending packets, which are typically voice packets, upstream (or return path) towards the Quad OIU 20A (operating in the central office) with the

HNU's source Media Access Control (MAC) address embedded in these packets. The packets from the particular HNU 50 are routed into the common FPGA 134 and stored in the SRAM 138. Each time the common FPGA 134 detects a new HNU 50, it interrupts the RISC processor 136, and the processor 136 goes out and learns the MAC address of the new HNU 50 so that the Quad OIU card 20A knows how to properly address downstream (or forward path) packets to that HNU 50 (e.g., See Paragraphs 0105; and 0108). The HNU 50 includes a RISC controller 158 to handle learning of the Quad OIU card address to route voice packets to that card correctly (e.g., See Paragraph 0114). Thus, the Kimbrough et al. publication discloses, at best, the actual addresses of Quad OIU card 20A and HNU 50 being respectively inserted into the downstream (or forward path) and upstream (or return path) packets, as opposed to an identifier for a downstream modulator at the headend facility that gets inserted into forward and reverse (or return path) packets and, from the reverse packet, converted to an IP address as recited in the independent claims.

Further, the Kimbrough et al. publication discloses that Ethernet PHY 54 is an integrated circuit that handles the physical layer transport of Ethernet packets to and from a subscriber data network (e.g., See Paragraph 0116). At the HNU 50, FPGA 150 extracts data packets (from electrical signals produced from received optical signals by Quplexer 52) and routes them to Ethernet PHY 54 for transmission to the subscriber data network. Upstream (or return path) signals from the Ethernet connection are packetized at the FPGA 150 and converted to optical signals for transmission to Quad OIU card 20A (e.g. See Paragraph 0120). Thus, the Ethernet PHY 54 (construed as the SWRD) merely serves as an Ethernet interface to the subscriber data

network. There is no disclosure, teaching or suggestion that the Ethernet PHY 54 converts an identifier of a headend modulator in a reverse (or return) path to an IP address of that modulator as recited in the claims. In fact, the Kimbrough et al. publication discloses that packetization (and presumably insertion of the actual destination address within these packets) for routing of return path packets from the subscriber data network to the Quad OIU card 20A is performed by FPGA 150, thereby indicating that the actual MAC address of the Quad OIU card 20A is not needed, or even known, by Ethernet PHY 54 (construed by the Examiner as the claimed SWRD) or devices connected thereto.

Accordingly, there is no disclosure, teaching or suggestion of identification of a downstream modulator at a headend facility from among a plurality of downstream modulators by transmitting in forward signals a modulator identification to the DHCT for insertion into the reverse header (carried in the reverse RF signals), and conversion (via demodulation of the reverse RF signals) of the modulator identification to an IP address to enable the reverse signals to be directed to the identified downstream modulator as recited by the independent claims.

Since the Farmer et al. patent and Kimbrough et al. publication do not disclose, teach or suggest, either alone or in combination, the features recited in independent claims 1 and 5 as discussed above, these claims are considered to be in condition for allowance.

Claims 2 - 4, 6, and 8 depend, either directly or indirectly, from independent claims 1 or 5 and, therefore, include all the limitations of their parent claims. The dependent claims are considered to be in condition for allowance for substantially the same reasons discussed above in relation to their parent claims, and for further limitations recited in the dependent claims.

In view of the foregoing, Applicants respectfully request the Examiner to find the application to be in condition for allowance with claims 1 - 6, and 8. However, if for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is respectfully requested to call the undersigned attorney to discuss any unresolved issues and to expedite the disposition of the application.

Applicants hereby petition for any extension of time that may be necessary to maintain the pendency of this application. The Commissioner is hereby authorized to charge payment of any additional fees required for the above-identified application or credit any overpayment to Deposit Account No. 05-0460.

Dated: 01/19/09

Respectfully submitted by:

/Stuart B. Shapiro/

Stuart B. Shapiro
Reg. No. 40169

EDELL, SHAPIRO & FINNAN, LLC
CUSTOMER NO.
1901 Research Boulevard, Suite 400
Rockville, MD 20850
(301) 424-3640